

| | Type | L # | Hits | Search Text | DBs | Time Stamp | Comments | Error Definition | Errors |
|---|------|-----|--------|------------------------------------------------------------------------------------------------|-------------------------------------------------------------------|---------------------|----------|------------------|--------|
| 1 | IS&R | L1 | 2 | ("20040110377").PN. | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | 2007/03/05 18:30 | | | |
| 2 | BRS | L2 | 103300 | (semiconductor or substrate) same stress\$2 | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | 2007/03/05 18:31 | | | |
| 3 | BRS | L3 | 67269 | (semiconductor or substrate) with stress\$2 | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | 2007/03/05 18:31 | | | |
| 4 | BRS | L4 | 13197 | (semiconductor or substrate) same (stress\$2 with prevent\$3) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | 2007/03/05 18:31 | | | |
| 5 | BRS | L5 | 9092 | (semiconductor or substrate) with (stress\$2 with prevent\$3) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | 2007/03/05 18:32 | | | |
| 6 | BRS | L6 | 500 | etch\$3 same ((semiconductor or substrate) with (stress\$2 with prevent\$3)) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | 2007/03/05 19:18 | | | |
| 7 | BRS | L7 | 328 | 6 and @pd<="20031114" | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | 2007/03/05 19:30 | | | |
| 8 | BRS | L8 | 578 | (etch\$3 same ((transistor or FET or gate) same (sidewall))) same (conformal with oxide) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | 2007/03/05 19:30 | | | |

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|----|------|-----|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------|---------------------|----------|------------------|--------|
| 9 | BRS | L9 | 396 | 8 and @pd<="20031114" | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | 2007/03/05 19:32 | | | |
| 10 | BRS | L10 | 269 | (etch\$3 same ((transistor or FET or gate) same (sidewall) same (source same drain))) same (conformal with oxide) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | 2007/03/05 20:34 | | | |
| 11 | BRS | L11 | 201 | 10 and @pd<="20031114" | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | 2007/03/05 20:40 | | | |
| 12 | BRS | L12 | 139 | (etch\$3 same (contact or opening or hole or node or nodal or sac or "self aligned")) same ((sidewall) same (source same drain) same (gate or electrode)) same (conformal with oxide) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | 2007/03/05 20:36 | | | |
| 13 | BRS | L13 | 106 | 12 and @pd<="20031114" | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | 2007/03/05 20:40 | | | |